Requested Patent: JP63280496A

Title: MANUFACTURE FOR MULTILAYER CIRCUIT BOARD ;

Abstracted Patent: JP63280496 ;

Publication Date: 1988-11-17 ;

Inventor(s): OGIWARA YOSHIAKI; SUDA HIDEO; SHIGA SHOJI; KONISHI SHINICHI ;

Applicant(s): FURUKAWA ELECTRIC CO LTD ;

Application Number: JP19870113517 19870512 ;

Priority Number(s): JP19870113517 19870512 ;

IPC Classification: H05K3/46 ;

Equivalents: ;

ABSTRACT:

PURPOSE:To suppress side etching to a minimum limit while to form a fine circuit with high accuracy and high density, by forming a mask member of predetermined pattern on the exposed surface of metal conductor foil and an electroplating layer on the surface of the metal conductor foil so that a conductor layer of various thicknesses is easily formed.

CONSTITUTION:A both-side metal conductor foil coated plate 3, after the perforation of a hole, activates the exposed surface by a Pd catalyst thereafter applies copper plating, forming an electroless-plated layer 5 on surfaces of metal conductor foils 2a, 2b containing inside a through hole 4 and a mask member 6, consisting of plating resist, in a predetermined region on both sides of the electroless-plated layer 5. Next, a thick thickness conductor part 13, comprising an electroplated layer 7, electroless-plated layer 5 and the metal conductor foil 2a, forms a circuit for large current use and a heat radiating part, and after removing the mask member 6, a thin thickness conductor part 11, comprising the electroless-plated layer 5 and the metal conductor foil 2a, forms a thin thickness circuit 8 in the predetermined part under a condition that the thick thickness conductor part 13 is protected. A both-size two-layered circuit board 15, thus obtained as described becomes the title circuit board independently.